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# Design and Implementation of 4-2 Compressor Design with New Xor-Xnor

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**Abstract:** In this paper, a low-power high speed 4:2 compressor circuit is proposed for fast digital arithmetic integrated circuits. The 4:2 compressor has been widely employed for multiplier realizations. Based on a new exclusive OR (XOR) and exclusive NOR (XNOR) module, a 4:2 compressor circuit has been designed. Proposed circuit shows power consumption is very less. Power consumption and delay of proposed 4-2 compressor circuit have been compared with earlier reported circuits and proposed circuit is proven to have the minimum power consumption and the lowest delay. Simulations have been performed by using verilog HDL.

**Keywords:** Full-Adder (FA), XOR-XNOR

## I. INTRODUCTION

Multipliers are one of the most significant blocks in computer arithmetic and are generally used in different digital signal processors. There is growing demands for high speed multipliers in different applications of computing systems, such as computer graphics, scientific calculation, image processing and so on. Speed of multiplier determines how fast the processors will run and designers are now more focused on high speed with low power consumption. The multiplier architecture consists of a partial product generation stage, partial product reduction stage and the final addition stage. The partial product reduction stage is responsible for a significant portion of the total multiplication delay, power and area. Therefore in order to accumulate partial products, compressors usually implement this stage because they contribute to the reduction of the partial products and also contribute to reduce the critical path which is important to maintain the circuit's performance.

Most computerized mathematic applications are executed utilizing digital logic circuits, in this manner working with a high degree of reliability and precision. In any case, numerous applications, for example, in multimedia and image processing can endure mistakes and imprecision in calculation and still produce important and helpful results. Exact and precise models and algorithm are not generally suitable or productive for use in these applications. The paradigm of inaccurate calculation depends on relaxing completely precise and totally deterministic building modules when for instance, planning energy efficient system.

This permits uncertain calculation to divert the current design procedure of computerized circuits and systems by exploiting a reduction in multifaceted nature and expense with conceivably a potential increment in execution and force productivity. In exact (or vague) figuring depends on utilizing this property to design disentangled, yet inexact circuits working at higher execution and/or lower power utilization contrasted and exact (definite) logic circuits.

Expansion and multiplication are broadly utilized operations as a part of computerized mathematic; for expansion adders and proposed a few new measurements for assessing rough and probabilistic adders as for brought together figures of legitimacy for outline appraisal for estimated processing applications. For every data to a circuit, the Error Distance(ED) is characterized as the mathematic separation between a mistaken yield and the right one. The Mean Error Distance (MED) and normalized error distance (NED) are proposed by considering the averaging impact of various inputs and the standardization of multiple-bit adders. The NED is almost invariant with the measure of an execution and is accordingly valuable in the unwavering quality evaluation of a particular configuration. The tradeoff in the middle of accuracy and force has additionally been quantitatively assessed in.

## II. COMPRESSOR

One of the major speed enhancement techniques used in modern digital circuits is the ability to add numbers with minimal carry propagation. The basic idea is that three numbers can be reduced to 2, in a 3:2 compressor, by doing the addition while keeping the carries and the sum separate.

This means that all of the columns can be added in parallel without relying on the result of the previous column, creating a two output "adder" with a time delay that is independent of the size of its inputs. The sum and carry can be recombined in a normal addition to form the correct

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result. This process may seem more complicated and pointless, but the power of this technique is that any amount, number of additions can be added together in this manner. It is only the final recombination of the final carry and sum that requires a carry propagating addition. 3:2 compressors is also known as full adder.

It adds three one bit binary numbers, a sum and a carry. The full adder is usually a component in a cascade of adders. The carry input for the full adder circuit is from the carry output from the cascade circuit. Carry output from full adder is fed to another full adder.

### III. 4-2 COMPRESSOR

A compressor is a device which is mostly used in multipliers to reduce the operands while adding terms of partial products. A typical M-N compressor takes M equally weighted input bits and produces N-bit binary number. The simplest and the most widely used compressor is the 3-2 compressor which is also known as a full adder. It has Three inputs to be summed up and provides two outputs. Similarly, a 4-2 compressor can also be built from two Cascaded 3-2 compressor circuits. The conventional implementation of a 4-2 compressor is composed of two serially connected full adders, as shown in fig.1. Different structures of 4-2 compressors are reported in literature and these are governing by the basic equation as Follows:

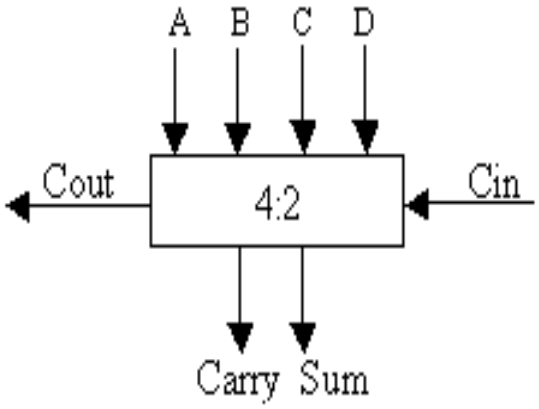


Fig 1 Block Diagram Of 4-2 compressor

One of the major speed enhancement techniques used in modern digital circuits is the ability to add numbers with minimal carry propagation. The basic idea is that three numbers can be reduced to 2, in a 3:2 compressor, by doing the addition while keeping the carries and the sum separate. This means that all of the columns can be added in parallel without relying on the result of the previous column, creating a two output "adder" with a time delay that is independent of the size of its inputs. The sum and carry can be recombined in a normal addition to form the correct result. This process may seem more complicated and pointless, but the power of this technique is that any amount, number of additions can beaded together in this manner. It is only the final recombination of the final carry and sum that requires a carry propagating addition. 3:2 compressor is also known as full adder. It adds three one bit binary numbers, a sum and a carry. The full adder is usually a component in a cascade of adders. The carry input for the full adder circuit is from the carry output from the cascade circuit. Carry output from full adder is fed to another full adder. The characteristics of the 4:2 compressors are:

- The outputs represent the sum of the five inputs, so it is really a 5 bit adder as shown in Fig.2.
- Both carries are of equal weighting (i.e. add "1" to the next column)
- To avoid carry propagation, the value of Cout depends only on A, B, C and D. It is independent of Cin.
- The Cout signal forms the input to the Cin of a 4:2 of the next column.

The common implementation of a 4-2 compressor is accomplished by utilizing two full-adder (FA) To add binary numbers cells.4:2 compressor is composed of two serially connected full adders. With minimal carry propagation we use compressor adder instead of other adder. Compressor is a digital modern circuit which is used for high speed with minimum gates requires designing technique. This compressor becomes the essential tool for fast multiplication adding technique on fast processor and lesser area.

A compressor is a device which is mostly used in multipliers to reduce the operands while adding terms of partial products. A typical M-N compressor takes M equally weighted input bits and produces N-bit binary number. The simplest and the most widely used compressor is the 3-2 compressor which is also known as a full adder. It has Three inputs to be summed up and provides two outputs. Similarly, a 4-2 compressor can also be built from two Cascaded 3-2 compressor circuits. The conventional implementation of a 4-2 compressor is composed of two serially connected full adders, as shown in fig.1. Different structures of 4-2 compressors are reported in literature and these are governing by the basic equation as Follows:

$$X1+X2+X3+X4+C_{in}=Sum+2\cdot(Carry+C_{out})$$

The common implementation of a 4-2 compressor is accomplished by utilizing two full-adder (FA) cells (Fig.2) [8]. Different designs have been proposed in the literature for 4-2 compressor. The optimized design of an exact4-2 compressor based on the so-called XOR-XNOR gates ;
a XOR-XNOR gate simultaneously generates the XOR and XNOR output signals. The design of consists of three XORXNOR (denoted by XOR*) gates, one XOR and two 2-1 MUX es. The critical path of this design has a delay of $3\Delta$, where $\Delta$ is the unitary delay through any gate in the design.

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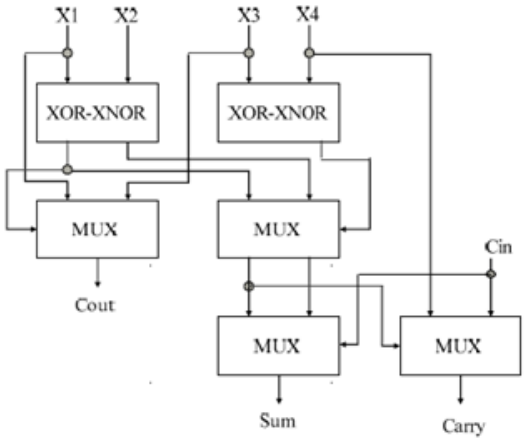


Fig.2. 4-2 compressor xor –xnor module

4:2 compressors are capable of adding 4 bits and one carry, in turn producing a 3 bit output. The 4-2 compressor has 4 inputs X1, X2, X3 and X4 and 2 outputs Sum and Carry along with a Carry-in (Cin) and a Carry-out (Cout). The input Cin is the output from the previous lower significant compressor. The Cout is the output to the compressor in the next significant stage. The critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders. However, like in the case of 3-2 compressor, the fact that both the output and its complement are available at every stage is neglected. Thus replacing some XOR blocks with multiplexer's results in a significant improvement in delay as shown in Fig.4. Also the MUX block at the SUM output gets the select bit before the inputs arrive and this minimizes the delay to a considerable extent.

## IV. MULTIPLICATION

In this section, the impact of using the proposed compressors for multiplication is investigated. A fast (exact) multiplier is usually composed of three parts (or modules) .

- Partial product generation
- A Carry Save Adder (CSA) tree to reduce the partial products' matrix to an addition of only two operands
- A Carry Propagation Adder (CPA) for the final computation of the binary result

In the design of a multiplier, the second module plays a pivotal role in terms of delay, power consumption and circuit complexity. Compressors have been widely used [9, 10] to speed up the CSA tree and decrease its power dissipation, so to achieve fast and low-power operation. The use of approximate compressors in the CSA tree of a multiplier results in an approximate multiplier.

### A. Wallace Tree Multiplier

Wallace Tree multiplier accumulates partial products column-wise into three and two bits and gives them to Full- Adders and Half Adders respectively to reduce as Sum, Carry bits. Any bit that does not belong to these adders are bypassed to next stage and carry is propagated to one-bit higher order column of next stage. Wallace accumulates as many bits as possible into adders [10]. At each stage, this process is continued until the stage height is reduced to 2 rows. The Wallace tree 8x8 multiplier along with its reduction stage .

## V. SIMULATION RESULTS

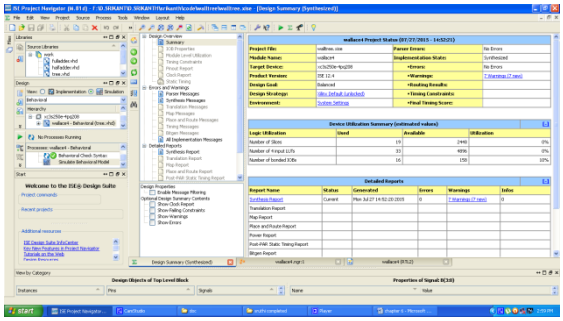

Fig 3 Synthasis Report

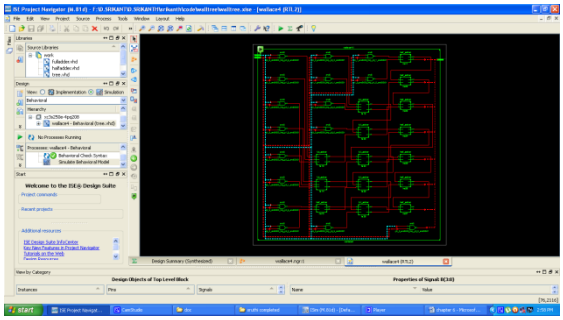

Fig 4 Schematic RTL

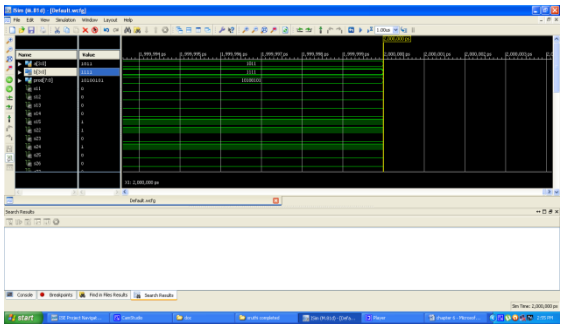

Fig 5 Schematic of 4:2 compressor using xor-xnor and mux

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